Amendments To The Specification

Please replace the paragraph beginning on page 6, line 14, of the original Application with the following paragraph:

"Now referring to FIGURE 3, a schematic diagram [[300]] shows a preferred embodiment 300 of [[a]] the pulse-limiting circuit 204 of FIGURE 2. The pulse-limiting circuit 300 generally comprises a first p-channel metal-oxide-silicon (PMOS) transistor 302, a second PMOS 304, a first n-channel metal-oxide-silicon (NMOS) transistor 306, a third PMOS 308, a fourth PMOS 310, a second NMOS 312, a third NMOS 314, a first inverter 316, a second inverter 318, a first delay block 320, a second delay block 322, a third delay block 324, a fourth delay block 326, a third inverter 328, and a fourth inverter 330. The delay block 320 includes four [[AND]] NAND gates 332, 334, 336, and 338 coupled in series. Similarly, the delay block 322 includes four [[AND]] NAND gates 340, 342, 344, and 346 coupled in series. The delay block 324 includes four [[AND]] NAND gates 348, 350, 352, and 354 coupled in series. The delay block 326 includes four [[AND]] NAND gates 356, 358, 360, and 362 coupled in series."

Please replace the paragraph beginning on page 9, line 29, of the original Application with the following paragraph:

"Now referring to FIGURE 4, a schematic diagram [[400]] shows an alternative embodiment 400 of [[a]] the pulse-limiting circuit of FIGURE 2. The pulse-limiting circuit 400 [[comprises]] receives an input clock signal 402, and includes a first transport delay 404, a second transport delay 406, a first NOT logic 408, a first one-shot logic 410, a second one-shot logic 412, a third one-shot logic 414, a first D flip-flop (DFF) 416, a second D flip-flop (DFF) 418, a fourth one-

shot logic 420, a first AND logic 422, a second AND logic 424, a third AND logic 426, a first OR logic 428, a second NOT logic 430, a second OR logic 432, a third NOT logic 434, a first NAND logic 436, and a second NAND logic 438."